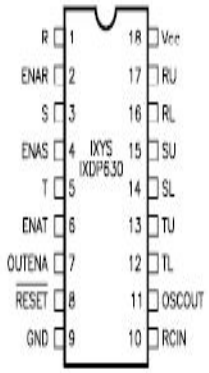
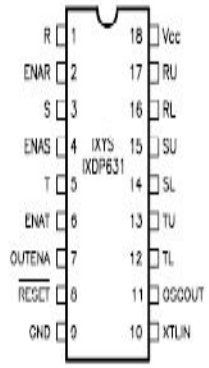
IXYS

IXDP630
IXDP631

Pin Description IXDP630



Pin Description IXDP631



Sym.	Pin	Description
R S T	1 3 5	R, S and T are the three single-phase inputs. Each input is expanded into two outputs to generate non-overlapping drive signals, RU/RL, SU/SL, and TU/TL. The delay from the falling edge of one line to the rising edge of the other is a function of the clock.
ENAR ENAS ENAT	2 4 6	High logic input will enable the outputs, as set by the proper input phase. The ENA (R,S,T) signals control the drive output lines. A low logic input will force both controlled outputs to a low logic level
OUT ENA	7	High logic level will enable all outputs to their related phase. The OUTENA simultaneously controls all outputs. Low input logic level will inhibit all outputs (low).
$\overline{\text{RESET}}$	8	The $\overline{\text{RESET}}$ signal is active low When a logic low $\overline{\text{RESET}}$ is applied, all outputs will go low. After releasing the $\overline{\text{RESET}}$ command within the generated delay, the outputs will align with the phase input level after the programmed delay internal.

Sym.	Pin	Description
GND	9	CIRCUIT GROUND - 0 Volts
RCIN or XTLIN	10	The first node of the clock network. For the IXDP630, the RC input is applied to RCIN. For the IXDP 631, the crystal oscillator is applied to XTLIN. If an external clock is to be supplied to the chip it should be connected to this pin.
OSC OUT	11	This is the output node of the oscillator. It is connected indirectly to the RCIN or XTLIN pins when using the internal oscillator as described in the applications information. It is not recommended for external use.
TL TU SL SU RL RU	12 13 14 15 16 17	After the appropriate delay, the external drive outputs (R,S, T) U are in phase with their corresponding inputs; (R,S, T) L are the complementary outputs.
V_{cc}	18	Voltage Supply +5 V ± 10 %

Agilent Technologies

Very High CMR, Wide V_{CC} Logic Gate Optocouplers

Technical Data

HCPL-2201 HCPL-2202
HCPL-2211 HCPL-2212
HCPL-2231 HCPL-2232
HCPL-0201 HCPL-0211
HCNW2201 HCNW2211

Features

- **10 kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 1000 V (HCPL-2211/2212/0211/2232, HCNW2211)**
- **Wide Operating V_{CC} Range: 4.5 to 20 Volts**
- **300 ns Propagation Delay Guaranteed over the Full Temperature Range**
- **5 Mbd Typical Signal Rate**
- **Low Input Current (1.6 mA to 1.8 mA)**
- **Hysteresis**
- **Totem Pole Output (No Pullup Resistor Required)**
- **Available in 8-Pin DIP, SOIC-8, Widebody Packages**
- **Guaranteed Performance from -40°C to 85°C**
- **Safety Approval**
  UL Recognized -2500 V rms for 1 minute (5000 V rms for 1 minute for HCNW22XX) per UL1577
  CSA Approved
  VDE 0884 Approved with V_{IORM} = 630 V peak (HCPL-2211/2212 Option 060 only) and V_{IORM} = 1414 V peak (HCNW22XX only)
- **MIL-STD-1772 Version Available (HCPL-52XX/62XX)**

Applications

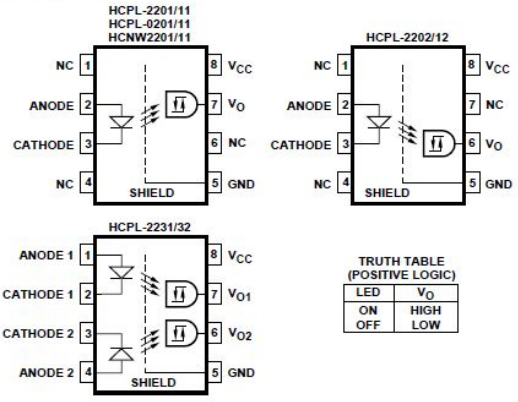
- **Isolation of High Speed Logic Systems**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **High Speed Line Receiver**
- **Power Control Systems**

Description

The HCPL-22XX, HCPL-02XX, and HCNW22XX are optically-coupled logic gates. The HCPL-22XX, and HCPL-02XX contain a GaAsP LED while the HCNW22XX contains an AlGaAs LED. The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic-compatible waveforms, eliminating the need for additional waveshaping.

A superior internal shield on the HCPL-2211/12, HCPL-0211,

Functional Diagram



TRUTH TABLE (POSITIVE LOGIC)

LED	V_O
ON	HIGH
OFF	LOW

A 0.1 µF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

HCF4050B

HEX BUFFER/CONVERTER (NON INVERTING)

- PROPAGATION DELAY TIME : t_{PD} = 40ns (TYP.) at V_{DD} = 10V C_L = 50pF
- HIGH TO LOW LEVEL LOGIC CONVERSION
- HIGH "SINK" AND "SOURCE" CURRENT CAPABILITY
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

DIP SOP

ORDER CODES

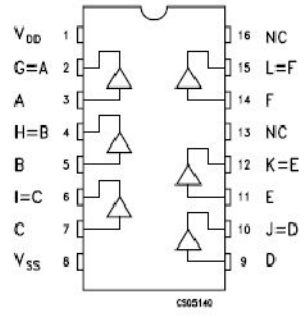
PACKAGE	TUBE	T & R
DIP	HCF4050BEY	
SOP	HCF4050BM1	HCF4050M013TR

DESCRIPTION

The HCF4050B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
It is an non inverting Hex Buffer/Converter and feature logic level conversions using only one supply voltage (V_{DD}).

The input high level signal (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. This device is intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads (V_{DD}=5V, V_{OL}≤0.4V and I_{OL}≤3.2mA.

PIN CONNECTION



Data Sheet No. PD60147 rev.U

International
IOR Rectifier

IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V or +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
  Separate logic supply range from 3.3V to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V_{OFFSET}	(IR2110)	500V max.
	(IR2113)	600V max.
I_O+/-		2A / 2A
V_{OUT}		10 - 20V
$t_{on/off}$ (typ.)		120 & 94 ns
Delay Matching	(IR2110)	10 ns max.
	(IR2113)	20ns max.

Packages

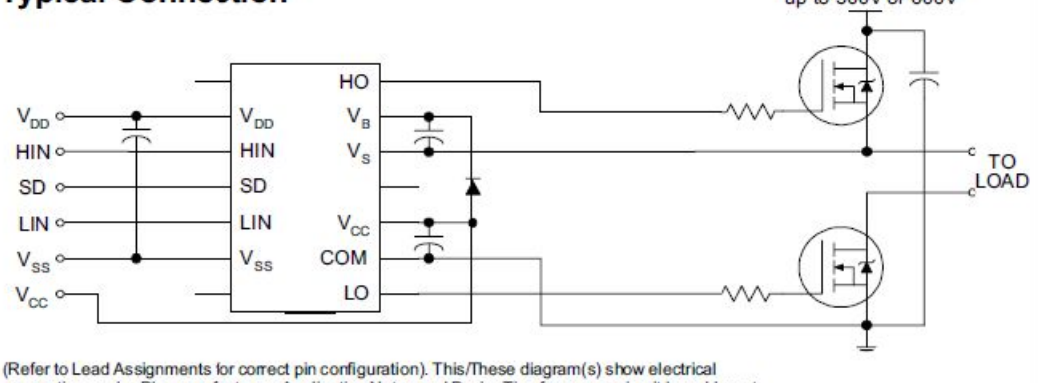
14-Lead PDIP
IR2110/IR2113

16-Lead SOIC
IR2110S/IR2113S

Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

SGS-THOMSON MICROELECTRONICS

IRF740
IRF740FI

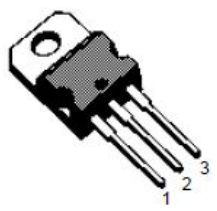
N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF740	400 V	< 0.55 Ω	10 A
IRF740FI	400 V	< 0.55 Ω	5.5 A

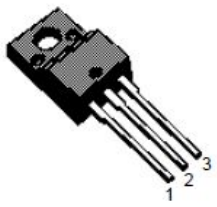
- TYPICAL $R_{DS(on)}$ = 0.42 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLIES (SMPS)
- CHOPPER REGULATORS, CONVERTERS, MOTOR CONTROL, LIGHTING FOR INDUSTRIAL AND CONSUMER ENVIRONMENT

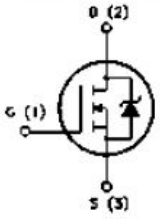


TO-220



ISOWATT220

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		IRF740	IRF740FI	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	400	400	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	400	400	V
V_{GS}	Gate-source Voltage	± 20		V
I_D	Drain Current (cont.) at T_c = 25 °C	10	5.5	A
I_D	Drain Current (cont.) at T_c = 100 °C	6.3	3	A
I_{DM}(•)	Drain Current (pulsed)	40	40	A
P_{tot}	Total Dissipation at T_c = 25 °C	125	40	W
	Derating Factor	1	0.32	W/°C
V_{ISO}	Insulation Withstand Voltage (DC)	—	2000	V
T_{stg}	Storage Temperature	-65 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

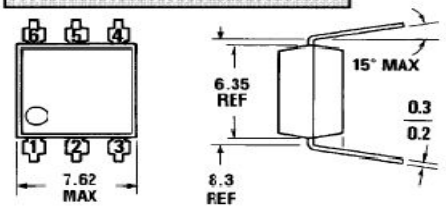
(•) Pulse width limited by safe operating area

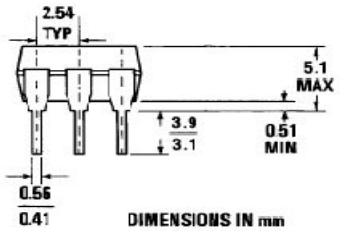
OPTOELECTRONICS

PHOTO SCR OPTOCOUPLERS

4N39 4N40

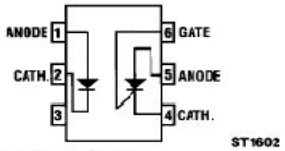
PACKAGE DIMENSIONS





DIMENSIONS IN mm
PACKAGE CODE E

ST1603



ST1602

Equivalent Circuit

DESCRIPTION

The 4N39 and 4N40 have a gallium-arsenide infrared emitting diode optically coupled with a light activated silicon controlled rectifier in a dual in-line package.

FEATURES & APPLICATIONS

- High efficiency, low degradation, liquid epitaxial LED
- 10 A, TTL compatible, solid state relay
- 25 W logic indicator lamp driver
- 400 V symmetrical transistor coupler
- Underwriters Laboratory (UL) recognized — File #E90700

ABSOLUTE MAXIMUM RATINGS

TOTAL PACKAGE

*Storage temperature ..... −55°C to 150°C
*Operating temperature ..... −55°C to 100°C
*Lead solder temperature ..... 260°C for 10 sec
*Total power dissipation (−55°C to 50°C) .. 450 mW
Derate linearly (above 50°C) ..... 9.0 mW/°C

INPUT DIODE

*Power dissipation (−55°C to 50°C) ..... 100 mW
Derate linearly (above 50°C) ..... 2 mW/°C
*Continuous forward current (−55°C to 50°C) 60 mA
*Peak forward current (−55°C to 50°C) ..... 1 A
*Reverse voltage (−55°C to 50°C) ..... 6 V

DETECTOR

*Power dissipation (−55°C to 50°C) ..... 400 mW
Derate linearly (above 50°C) ..... 8 mW/°C
*Off-state and reverse voltage 4N39 ..... 200 V
*(−55°C to +100°C) 4N40 ..... 400 V
*Peak reverse gate voltage (−55°C to 50°C) ..... 6 V
*Direct on-state current (−55°C to 50°C) .... 300 mA
*Surge on-state current (−55°C to 50°C) (100μS) 10 A
*Peak gate current (−55°C to 50°C) ..... 10 mA

*Indicates JEDEC Registered Data